## ANDES SCALES UP ITS RISC-V

*By Bob Wheeler (February 1, 2021)*

Andes converged its superscalar RISC-V CPU with multicore scaling to create its most powerful cluster to date. The AX45MP targets high-performance applications across diverse markets such as AR/VR, edge AI, automotive infotainment and ADAS, video processing, networking, and storage. Andes claims multiple design wins, having released initial RTL to customers in 3Q20; it expects general availability during 1H21. In addition to the 64-bit AX45MP, the 45-series includes the 32-bit A45MP. The company's new flagship RISC-V core competes with SiFive's U74MC, which preceded it by about two years.

At the cluster level, the A45MP and AX45MP are similar to the scalar A25MP and AX25MP cores that Andes announced in 2019 (see *MPR 4/15/19,* "Andes Strengthens Its RISC-V Arsenal"). The MP cluster combines up to four CPUs with a coherence manager and L2-cache controller, providing a 128-bit AXI-master interface to the rest of the SoC. The coherence manager implements a directory-based protocol, replacing the snooping protocol of the 25-series MP cores. It also presents an AXI-128 slave port for I/O, twice the width of the 25-series. Each CPU has an AXI-slave port for local memory. The MP cluster also includes debug support and a platform-level interrupt controller (PLIC).

The 45-series comprises the company's first superscalar CPUs, and they extend the pipeline to eight stages compared with five in the 25-series. The CPUs implement dynamic branch prediction with a 256-entry branch target buffer. As in the SiFive 7-series, the in-order pipeline includes two "late" ALUs to eliminate load-use penalties (see *MPR 11/12/18,* "SiFive Raises RISC-V Performance"). Using this approach, a dependent ALU instruction can issue in the same cycle as the instruction that loads its data. The separate two-cycle multiplier is fully pipelined. Andes rates the AX45 at 5.50 CoreMarks per megahertz, a 56% boost relative to the AX25. The CPU achieves a worst-case clock speed of 1.2GHz in 28nm technology and a typical 2.4GHz in 12nm technology.

The 45-series provides a set of performance improvements, which Andes brands MemBoost, that first appeared in the NX27V with vector (RVV) extensions (see *MPR 5/25/20,* "Andes Plots RISC-V Vector Heading"). They include instruction and data prefetch, multiple outstanding data accesses, and a dynamic write policy that enables cache bypass. To handle virtual memory, the A45 and AX45 have an MMU with a shared TLB that's configurable from 32 to 512 entries. They also offer physical-memory protection (PMP) with 16 regions. Customers can configure AX45 physical addressing (PA) as 38 bits (SV39) or 47 bits (SV48), whereas the A45 is limited to 34-bit PA (16GB).

The AX45MP competes most directly with SiFive's U74MC, another 64-bit RISC-V multicore cluster with L2-cache support and SMP-Linux compatibility. Although the CPU pipelines are similar, SiFive rates its design at a lesser 5.1 CoreMarks per megahertz, and it requires 7nm technology to achieve a 2.3GHz typical clock speed. We believe the AX45 and U74 have similar areas, so Andes should have the edge in CoreMarks per square millimeter. On the other hand, the U74MC scales to a maximum of nine CPUs, and SiFive allows customers to mix application CPUs and real-time CPUs in a cluster. The AX45 is unique in supporting both local memory (TCM) and a data cache, whereas SiFive customers must select one or the other. The core's 47-bit PA option is also unique, but we expect only designs implementing a multichip coherent interconnect will require more than 38 bits (256GB).

Although SiFive is rightly perceived as a RISC-V pioneer, Andes was the first established CPU-intellectual-property vendor to adopt the instruction set. Over the past several years, it expanded its RISC-V offering from microcontroller cores to embedded cores with DSP, vector, and floating-point units. The AX45 entered the same class as Arm's "little" Cortex-A55. Recent RISC-V design wins include Renesas IoT chips, Picocom's 5G-baseband processor, and several unnamed AI accelerators using NX27V cores. The AX45MP delivers an area-efficient midrange cluster suitable for SMP Linux, enabling SoC designs that were previously beyond Andes' reach. ♦